WHAT IS CLAIMED IS:

1. A semiconductor integrated circuit comprising:

a memory cell capable of forming an electrical path with a predetermined potential selectively by a stored information voltage;

a first data line for outputting the information stored in said memory cell;

a second data line paired with said first data line; and

a precharge circuit for precharging said first data line to a first precharge potential and precharging said second data line to a second precharge potential different from said first precharge potential.

2. A semiconductor integrated circuit according to Claim 1,

wherein said first data line has a hierarchical structure including a plurality of first local data lines and a first global data line, said hierarchical structure being configured with a plurality of blocks each including a predetermined number of said memory cells connected to corresponding one of said plurality of first local data lines, said blocks being selectively connected to said first global data lines by a control signal; and

wherein said plurality of first local data lines and said first global data line are arranged in

parallel to each other on a memory array using different metal wiring layers.

3. A semiconductor integrated circuit according to Claim 1,

wherein said first data line has a hierarchical structure including a plurality of first local data lines and a first global data line, said hierarchical structure being configured with a plurality of blocks each including a predetermined number of said memory cells connected to corresponding one of said plurality of first local data lines, said blocks being selectively connected to said first global data line by a control signal; and

wherein said second data line has a hierarchical structure having a plurality of second local data lines paired with said plurality of first local data lines, respectively, and a second global data line paired with said first global data line, respectively, said hierarchical structure being configured with a plurality of blocks each including a predetermined number of said memory cells connected to corresponding one of said plurality of second local data lines, said blocks being selectively connected to said second global data line by a control signal:

wherein said precharge circuit is arranged for said plurality of first local data lines and said plurality of second local data lines paired with each other; and

said plurality of first local data lines and said plurality of second local data lines are wired using a first metal wiring layer, and said first global data line and said second global data line are wired using a second metal wiring layer.

4. A semiconductor integrated circuit according to Claim 3, further includes: an amplifier for amplifying signals on said first and second data lines or signal voltages on said first and second global data lines.

5. A semiconductor integrated circuit according to Claim 3,

wherein said memory cell is able to make an electrical path to a first potential lower than a second potential selectively by a stored information voltage; and

wherein said first precharge potential is higher than said second precharge potential.

6. A semiconductor integrated circuit according to Claim 5, further includes: an amplifier for amplifying signals on said first and second data lines or signal voltages on said first and second global data lines to said first potential or said second potential; and

wherein said first precharge potential is higher than said second precharge potential at least by a sensitivity voltage Δ constituting a minimum potential difference that can be detected by said

amplifier.

7. A semiconductor integrated circuit according to Claim 5,

wherein said first precharge potential is said first potential, and said second precharge potential is a third potential approximately one half in value between said first potential and said second potential.

8. A semiconductor integrated circuit according to Claim 3,

wherein said memory cell is able to make an electrical path to a second potential higher than said first potential selectively by a stored information voltage, and said first precharge potential is lower than said second precharge potential.

9. A semiconductor integrated circuit according to Claim 8, further including an amplifier for amplifying signals on said first and second data lines or signal voltages on said first and second global data lines; and

wherein said first precharge potential is lower than said second precharge potential by at least a sensitivity voltage Δ constituting a minimum potential difference that can be detected by said amplifier.

10. A semiconductor integrated circuit according to Claim 8,

wherein said first precharge potential is

said first potential, and said second precharge potential is a third potential one half in value between said first potential and said second potential.

11. A semiconductor integrated circuit according to Claim 2,

wherein said first data lines have a hierarchical structure and have a precharge circuit for each of said blocks.

12. A semiconductor integrated circuit according to Claim 3,

wherein said precharge circuit includes a plurality of unit precharge circuits corresponding to each of said plurality of first and second local data lines.

13. A semiconductor integrated circuit according to Claim 12, further including a second precharge circuit for precharging said first and second global data lines to a common potential.

14. A semiconductor integrated circuit according to Claim 2,

wherein said global data lines are twisted with each other on a memory mat.

15. A semiconductor integrated circuit according to Claim 4,

wherein the information stored in said memory cell is amplified by said amplifier in such a manner that said plurality of first and second local data lines are electrically isolated from said first and

second global data lines by a control signal for connecting said plurality of first and second local data lines and said first and second global data lines in order to attain an electrical balance between said first and second global data lines.

16. A semiconductor integrated circuit according to Claim 1,

wherein said memory cell includes a first transistor for holding the information voltage at the gate thereof and turned on/off in accordance with said information voltage, a second transistor for applying a write signal to the gate of said first transistor, and a third transistor for outputting as a read signal the information in on state or in off state in accordance with the information voltage for the gate of said second transistor.

17. A semiconductor integrated circuit according to Claim 16, further comprising a word line connected to a control node of said second transistor and a control terminal of said third transistor of said memory cell,

wherein said first data line has a hierarchical structure including a plurality of first data lines and a first global data line, and said second data line has a hierarchical structure including a plurality of second data lines and a second global data line,

wherein said word line has a first select

period during which said word line is set to a first voltage, and said third transistor and said second transistor are turned off regardless of said information voltage in unselect mode, while said third transistor is turned on and said second transistor is kept off in read select mode, and a second select period during which said word line is set to a second voltage, and said third transistor and said second transistor for writing the write data transmitted to one of said plurality of second local data lines in said memory cell are turned on at the same time in write select mode,

wherein said plurality of first and second local data lines are arranged in parallel to said first and second global data lines connected to an amplifier for amplifying the information stored in said memory cell,

wherein one of said plurality of first local data lines and said first global data line is connected to each other by a read and transfer transistor, one of said plurality of second local data lines and said second global data line is connected to each other by a write and transfer transistor,

wherein at the time of the read operation from said memory cell, one of said plurality of first local data lines are connected to said first global data line using a read control transistor, the data read from said memory cell during the first select

period of said word line are transmitted to said first global data line by turning on said read control transistor and amplified by an amplifier with the voltage of said second global data line as a reference voltage, and

wherein at the time of the write operation to said memory cell, one of said plurality of second data lines is connected to said second global data line using said write and transfer transistor, and the write data transmitted to said second global data line during said second select period of said word line are transmitted to the one of said plurality of second local data lines.

18. A semiconductor integrated circuit according to Claim 4,

wherein said amplifier amplifies the signal voltages on said first and second global data lines to selected one of a first potential and a second potential, and

wherein during the precharge period of said semiconductor integrated circuit, said plurality of first local data lines are precharged to said second voltage, and said plurality of second local data lines and said first and second global data lines are precharged to a third potential constituting a substantially intermediate voltage between said first potential and said second potential.

19. A semiconductor integrated circuit according

to Claim 18,

wherein said memory cell includes a first transistor for holding an information voltage at the gate thereof and turned on or off in accordance with said information voltage, a second transistor for applying a write signal to the gate of said first transistor, and a third transistor for outputting as a read signal the information in on state or in off state in accordance with said information voltage to the gate of said second transistor.

20. A semiconductor integrated circuit according to Claim 4,

wherein said amplifier includes a differential amplifier circuit.

21. A semiconductor integrated circuit according to Claim 20,

wherein said differential amplifier circuit includes a CMOS latch circuit having a pair of CMOS inverter circuits with the input and output terminals thereof connected by being twisted with each other.

22. A semiconductor integrated circuit according to Claim 16,

wherein said second transistor is a second MOSFET and said third transistor is a third MOSFET, and the gate electrodes of said second MOSFET and said third MOSFET are connected to a word line.

23. A semiconductor integrated circuit according to Claim 22,

wherein said first transistor is a N-type first MOSFET.

24. A semiconductor integrated circuit according to Claim 23,

wherein said first voltage is set during said first select period for the read operation from said memory cell on condition that said first voltage has a value higher than the threshold value Vtr of said third MOSFET, smaller than the sum of the threshold value Vtw of said second MOSFET and the precharge voltage of said plurality of second local data lines and smaller than the sum of the threshold value Vtw of said second MOSFET and the threshold value Vts of said first MOSFET.

25. A semiconductor integrated circuit according to Claim 23,

wherein said second voltage is set during said second select period for the write operation into said memory cell on condition that said second voltage has a value equal to or larger than the sum of the threshold value Vtqw of said second MOSFET and the source voltage VDD.